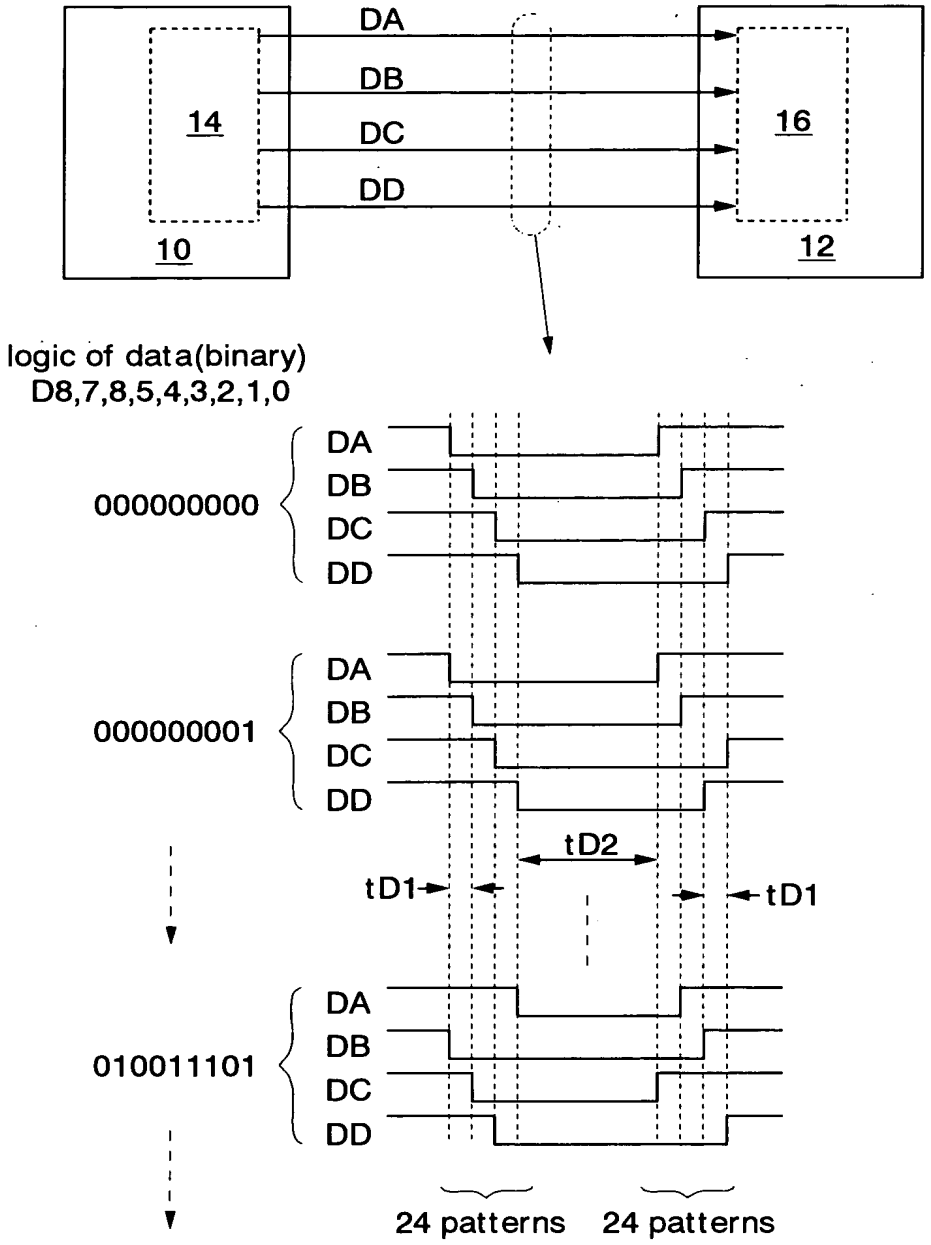

DA
DB
DC
DD
14
16
10
12
logic of data(binary)
D8,7,8,5,4,3,2,1,0
000000000
000000001
010011101
tD1
tD2
tD1
24 patterns
24 patterns

Fig. 1

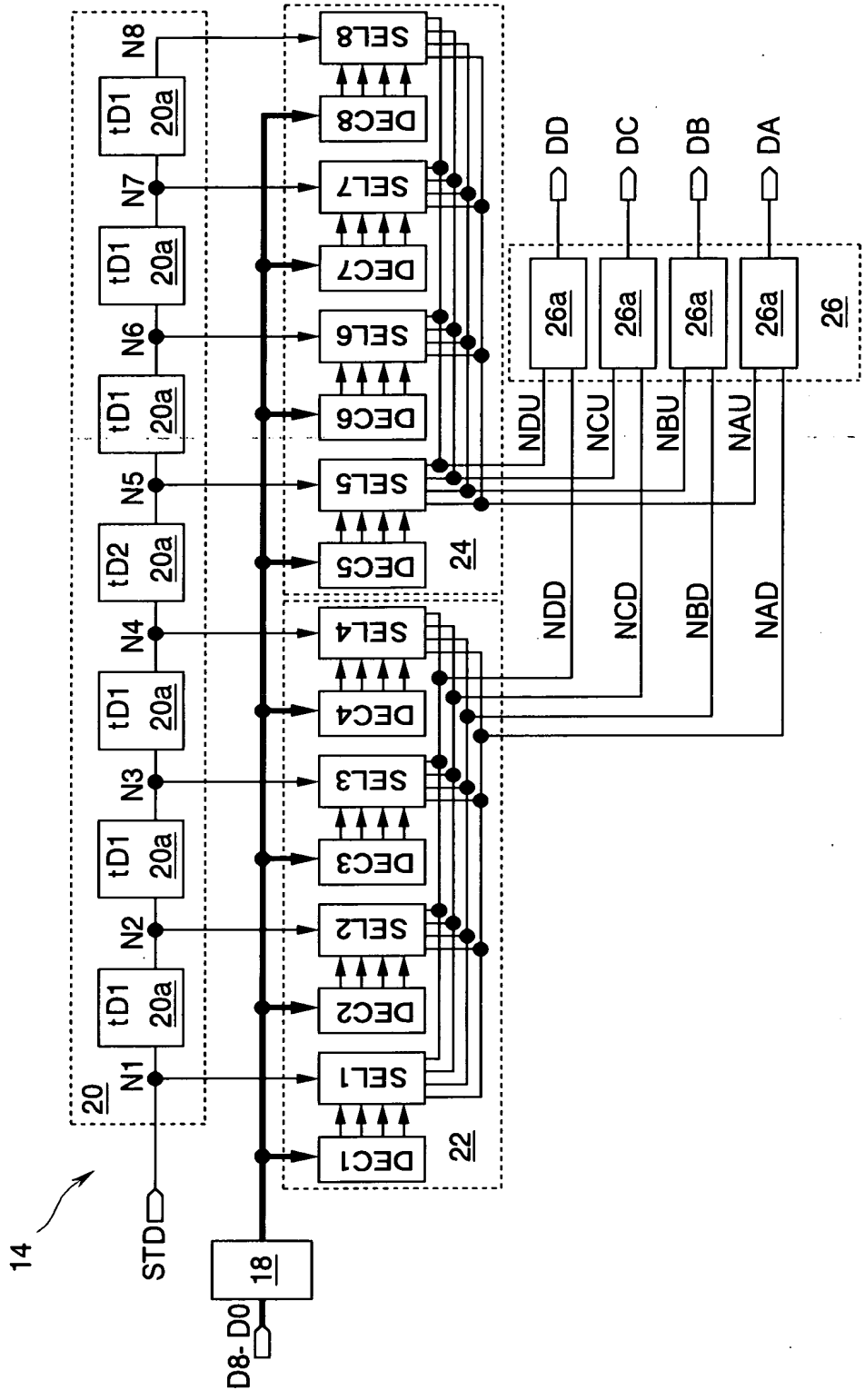

14
STD
D8-D0
18
20
22
24
26
N1
N2
N3
N4
N5
N6
N7
N8
tD1
tD2
20a
SEL1
SEL2
SEL3
SEL4
SEL5
SEL6
SEL7
SEL8
DEC1
DEC2
DEC3
DEC4
DEC5
DEC6
DEC7
DEC8
26a
DA
DB
DC
DD
NAD
NBD
NCD
NDD
NAU
NBU
NCU
NDU

Fig. 2

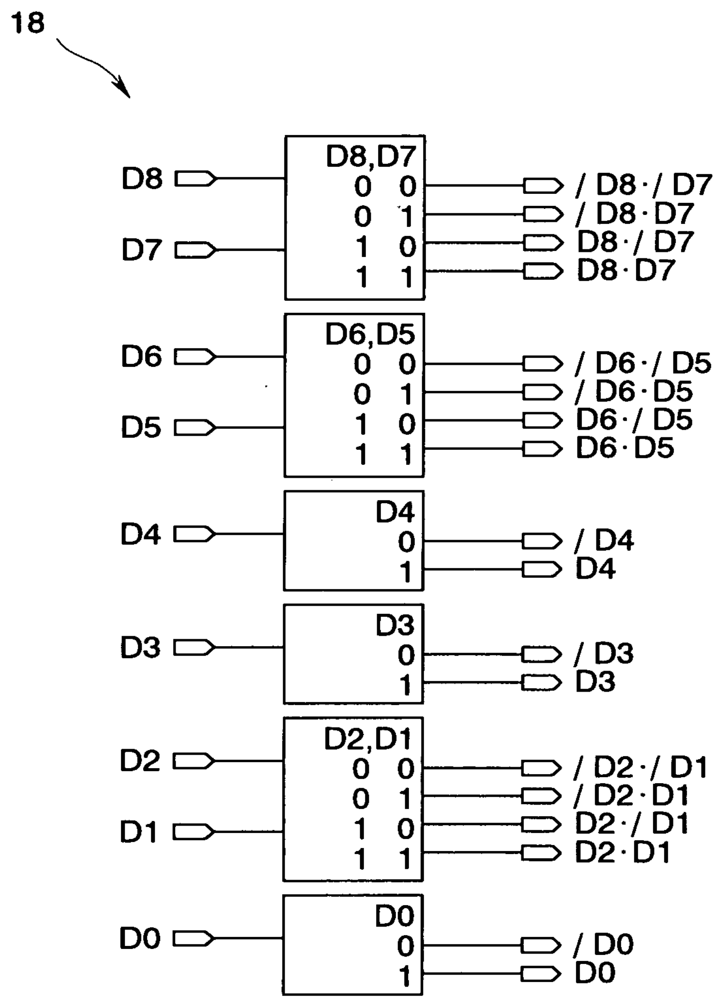

18
D8
D7
D8,D7
0 0
0 1
1 0
1 1
/ D8·/ D7
/ D8·D7
D8·/ D7
D8·D7
D6
D5
D6,D5
0 0
0 1
1 0
1 1
/ D6·/ D5
/ D6·D5
D6·/ D5
D6·D5
D4
0
1
/ D4
D4
D3
0
1
/ D3
D3
D2
D1
D2,D1
0 0
0 1
1 0
1 1
/ D2·/ D1
/ D2·D1
D2·/ D1
D2·D1
D0
0
1
/ D0
D0

Fig. 3

		for leading edge							for trailing edge				
		logic L1			logic L2								
No.	order of edges	D8,7	D6,5	D4	D8,7	D6,5	D4	D3	D8,7	D3	D2,1	D0	
0	ABCD	00	00	0	11	00	0	0	11bar	0	00	0	logic L1
1	ABDC	00	00	1	11	00	1	0	11bar	0	00	1	
2	ACBD	00	01	0	11	01	0	0	11bar	0	01	0	
3	ACDB	00	01	1	11	01	1	0	11bar	0	01	1	
4	ADBC	00	10	0	11	10	0	0	11bar	0	10	0	
5	ADCB	00	10	1	11	10	1	0	11bar	0	10	1	
6	BACD	00	11	0	11	11	0	0	11bar	0	11	0	
7	BADC	00	11	1	11	11	1	0	11bar	0	11	1	
8	BCAD	01	00	0	11	00	0	1	11bar	1	00	0	
9	BCDA	01	00	1	11	00	1	1	11bar	1	00	1	
10	BDAC	01	01	0	11	01	0	1	11bar	1	01	0	
11	BDCA	01	01	1	11	01	1	1	11bar	1	01	1	
12	CABD	01	10	0	11	10	0	1	11bar	1	10	0	
13	CADB	01	10	1	11	10	1	1	11bar	1	10	1	
14	CBAD	01	11	0	11	11	0	1	11bar	1	11	0	
15	CBDA	01	11	1	11	11	1	1	11bar	1	11	1	
16	CDAB	10	00	0					11	-	00	0	logic L2
17	CDBA	10	00	1					11	-	00	1	
18	DABC	10	01	0					11	-	01	0	
19	DACB	10	01	1					11	-	01	1	
20	DBAC	10	10	0					11	-	10	0	
21	DBCA	10	10	1					11	-	10	1	
22	DCAB	10	11	0					11	-	11	0	
23	DCBA	10	11	1					11	-	11	1	

Fig. 4

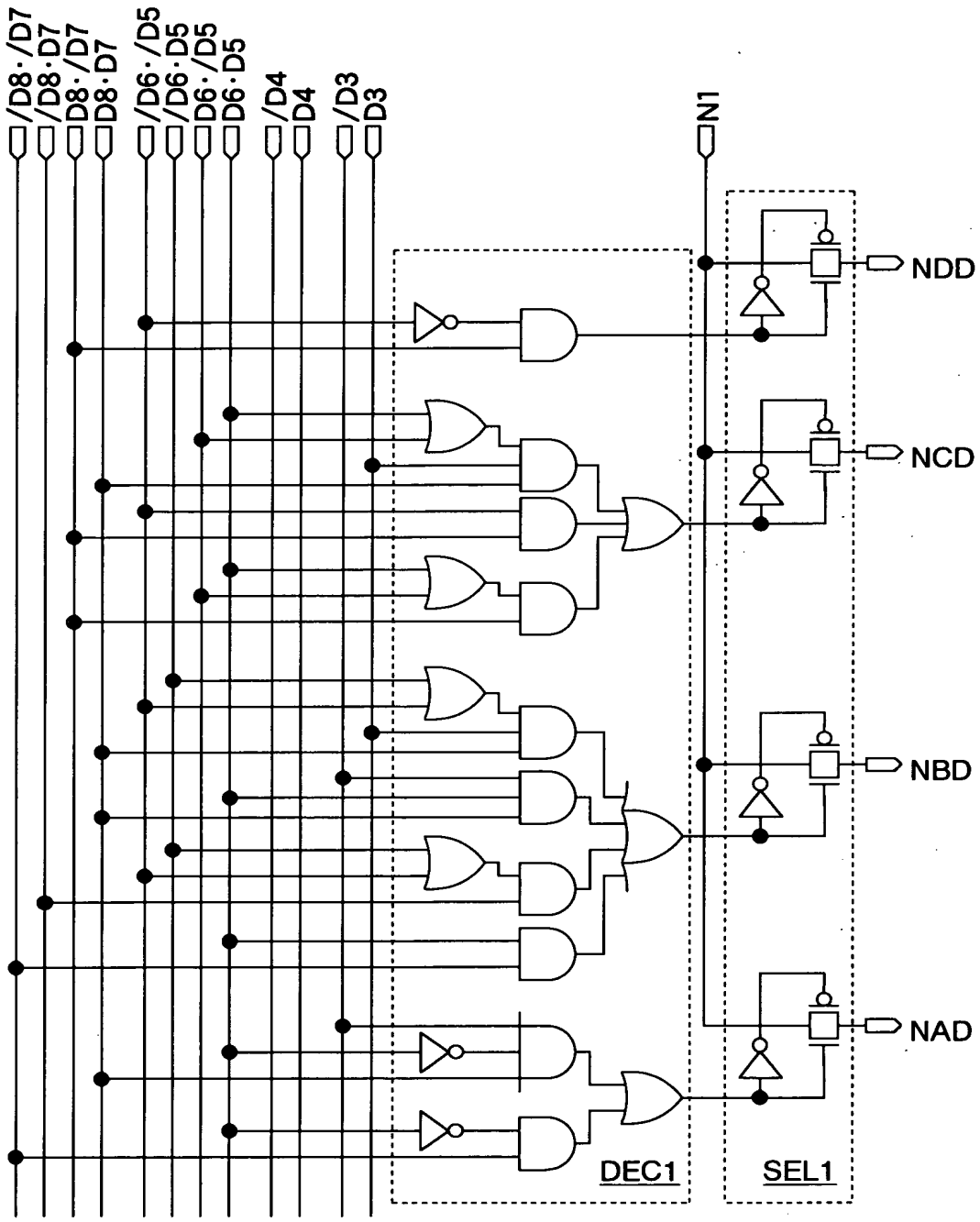

/D8·/D7
/D8·D7
D8·/D7
D8·D7
/D6·/D5
/D6·D5
D6·/D5
D6·D5
/D4
D4
/D3
D3
N1
NDD
NCD
NBD
NAD
DEC1
SEL1

Fig. 5

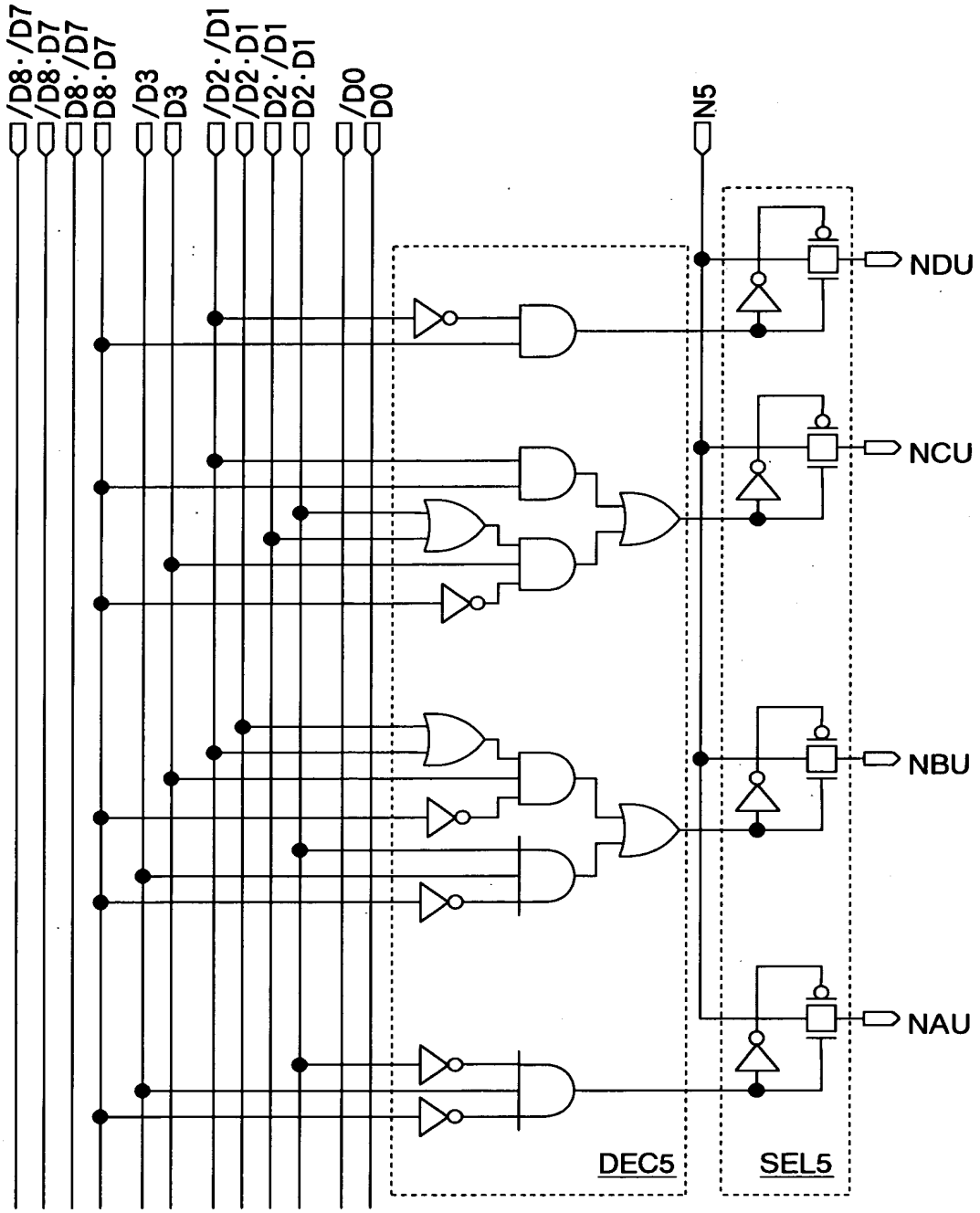

/D8·/D7
/D8·D7
D8·/D7
D8·D7
/D3
D3
/D2·/D1
/D2·D1
D2·/D1
D2·D1
/D0
D0
N5
NDU
NCU
NBU
NAU
DEC5
SEL5

Fig. 6

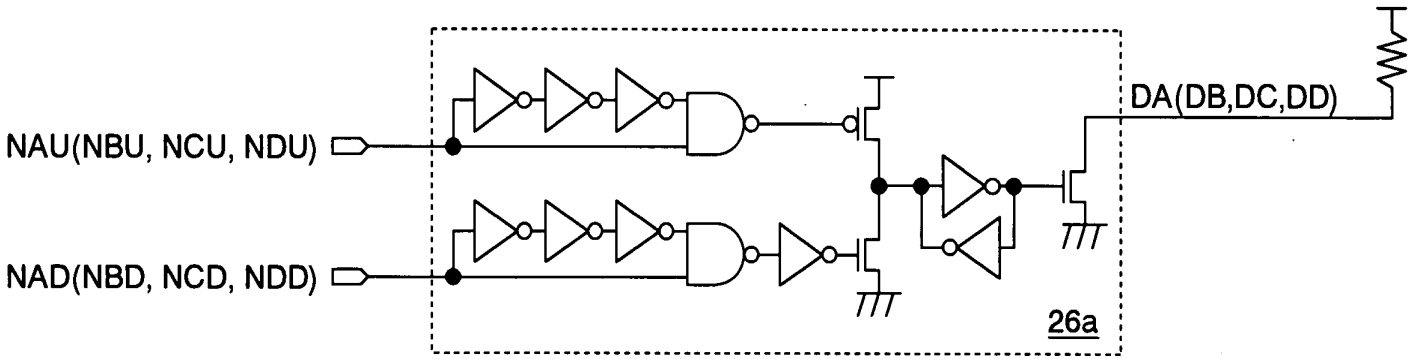
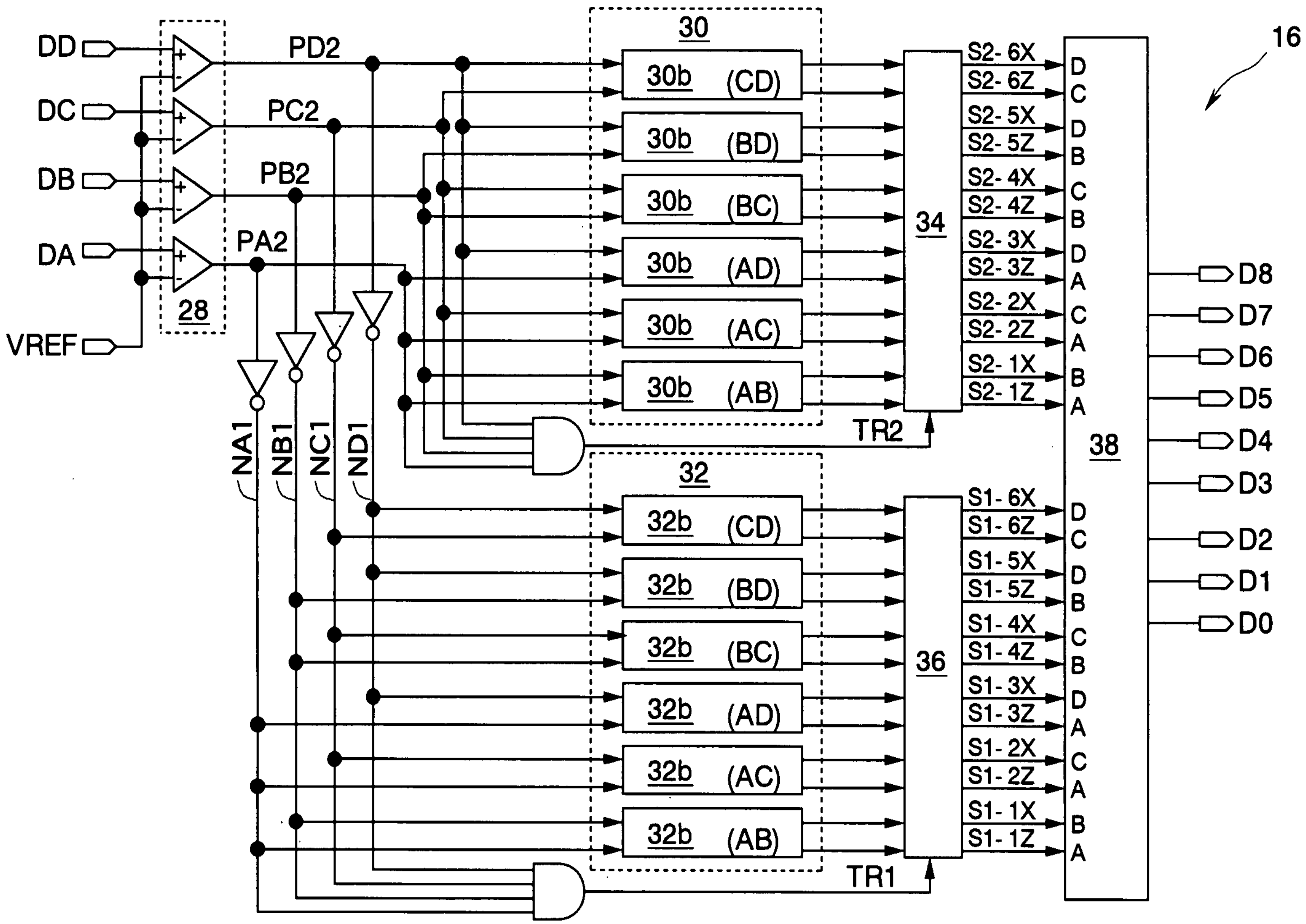


Fig. 7



DD
DC
DB
DA
VREF
28
PD2
PC2
PB2
PA2
NA1
NB1
NC1
ND1
30
30b (CD)
30b (BD)
30b (BC)
30b (AD)
30b (AC)
30b (AB)
32
32b (CD)
32b (BD)
32b (BC)
32b (AD)
32b (AC)
32b (AB)
TR2
TR1
34
36
S2-6X
S2-6Z
S2-5X
S2-5Z
S2-4X
S2-4Z
S2-3X
S2-3Z
S2-2X
S2-2Z
S2-1X
S2-1Z
S1-6X
S1-6Z
S1-5X
S1-5Z
S1-4X
S1-4Z
S1-3X
S1-3Z
S1-2X
S1-2Z
S1-1X
S1-1Z
38
D8
D7
D6
D5
D4
D3
D2
D1
D0
16

Fig. 8

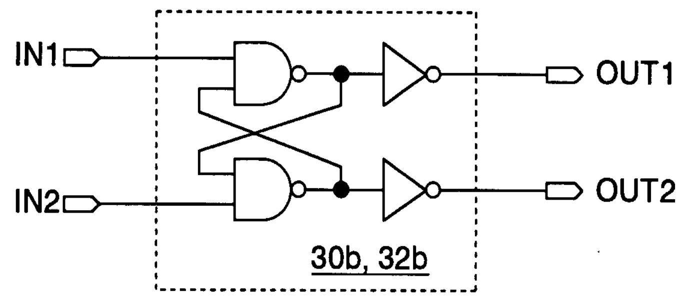


Fig. 9

		for leading edge							for trailing edge					
No.	order of edges	output OUT of comparator 32b 1,2,3,4,5,6	logic L1 D8,7	logic L1 D6,5	logic L1 D4	logic L2 D8,7	logic L2 D6,5	logic L2 D4	logic L2 D3	output OUT of comparator 30b 1,2,3,4,5,6	D8,7	D3	D2,1	D0	
0	ABCD	111111	00	00	0	11	00	0	0	111111	11bar	0	00	0	logic L1
1	ABDC	111110	00	00	1	11	00	1	0	111110	11bar	0	00	1	
2	ACBD	111011	00	01	0	11	01	0	0	111011	11bar	0	01	0	
3	ACDB	111001	00	01	1	11	01	1	0	111001	11bar	0	01	1	
4	ADBC	111100	00	10	0	11	10	0	0	111100	11bar	0	10	0	
5	ADCB	111000	00	10	1	11	10	1	0	111000	11bar	0	10	1	
6	BACD	011111	00	11	0	11	11	0	0	011111	11bar	0	11	0	
7	BADC	011110	00	11	1	11	11	1	0	011110	11bar	0	11	1	
8	BCAD	001111	01	00	0	11	00	0	1	001111	11bar	1	00	0	
9	BCDA	000111	01	00	1	11	00	1	1	000111	11bar	1	00	1	
10	BDAC	010110	01	01	0	11	01	0	1	010110	11bar	1	01	0	
11	BDCA	000110	01	01	1	11	01	1	1	000110	11bar	1	01	1	
12	CABD	101011	01	10	0	11	10	0	1	101011	11bar	1	10	0	
13	CADB	101001	01	10	1	11	10	1	1	101001	11bar	1	10	1	
14	CBAD	001011	01	11	0	11	11	0	1	001011	11bar	1	11	0	
15	CBDA	000011	01	11	1	11	11	1	1	000011	11bar	1	11	1	
16	CDAB	100001	10	00	0					100001	11	-	00	0	logic L2
17	CDBA	000001	10	00	1					000001	11	-	00	1	
18	DABC	110100	10	01	0					110100	11	-	01	0	
19	DACB	110000	10	01	1					110000	11	-	01	1	
20	DBAC	010100	10	10	0					010100	11	-	10	0	
21	DBCA	000100	10	10	1					000100	11	-	10	1	
22	DCAB	100000	10	11	0					100000	11	-	11	0	
23	DCBA	000000	10	11	1					000000	11	-	11	1	

Fig. 10

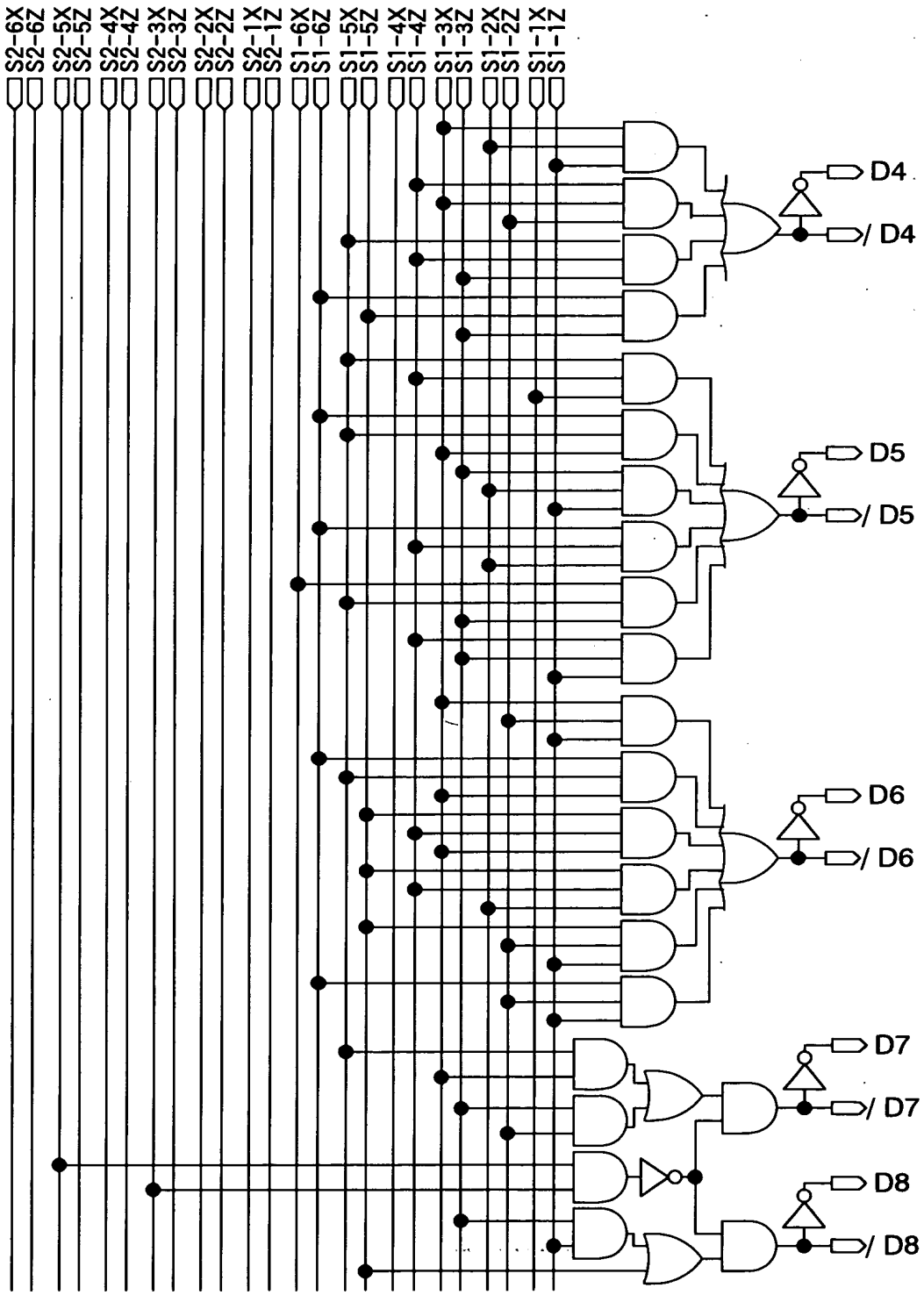

S2-6X
S2-6Z
S2-5X
S2-5Z
S2-4X
S2-4Z
S2-3X
S2-3Z
S2-2X
S2-2Z
S2-1X
S2-1Z
S1-6X
S1-6Z
S1-5X
S1-5Z
S1-4X
S1-4Z
S1-3X
S1-3Z
S1-2X
S1-2Z
S1-1X
S1-1Z
D4
/ D4
D5
/ D5
D6
/ D6
D7
/ D7
D8
/ D8

Fig. 11

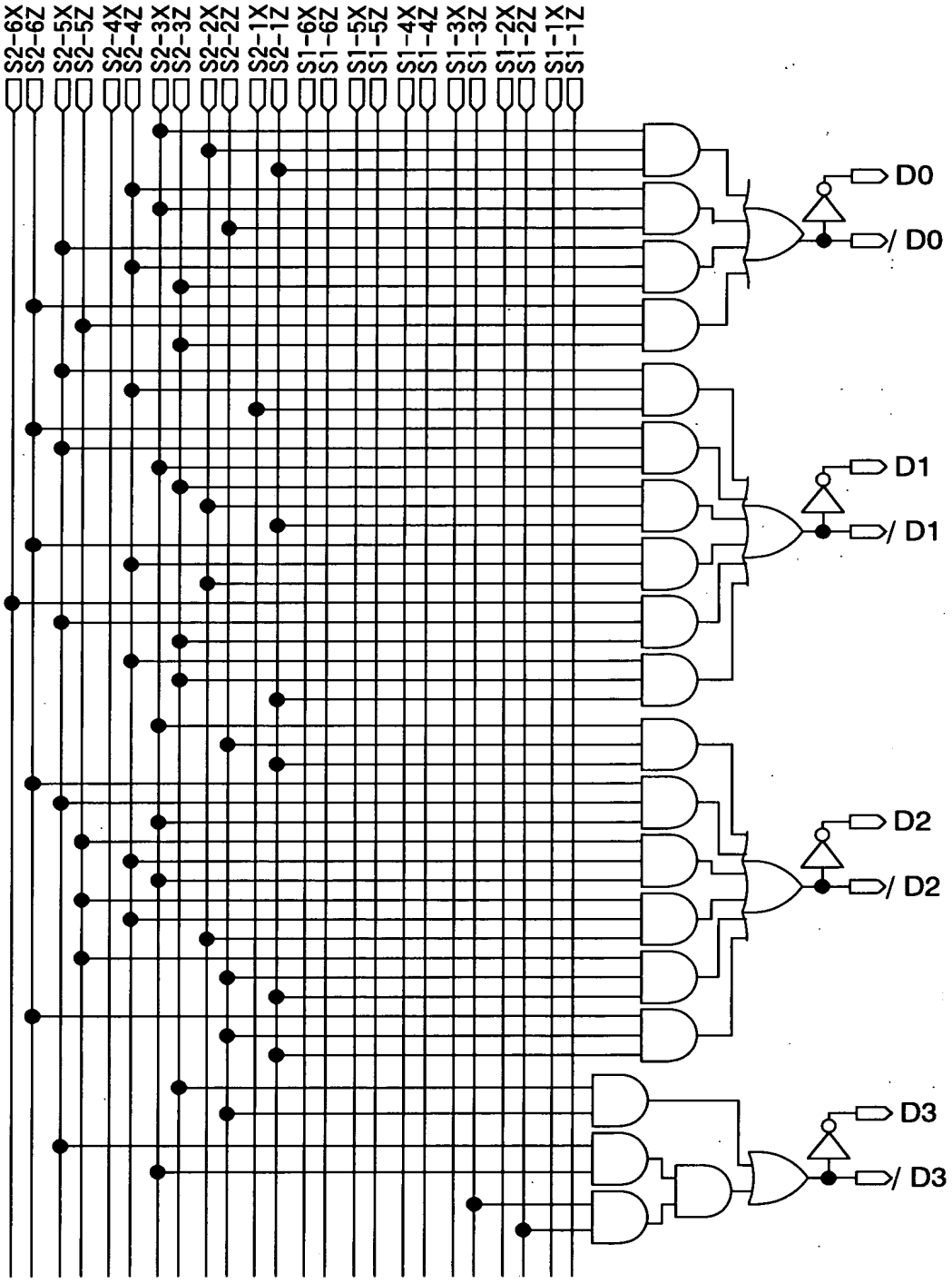


Fig. 12

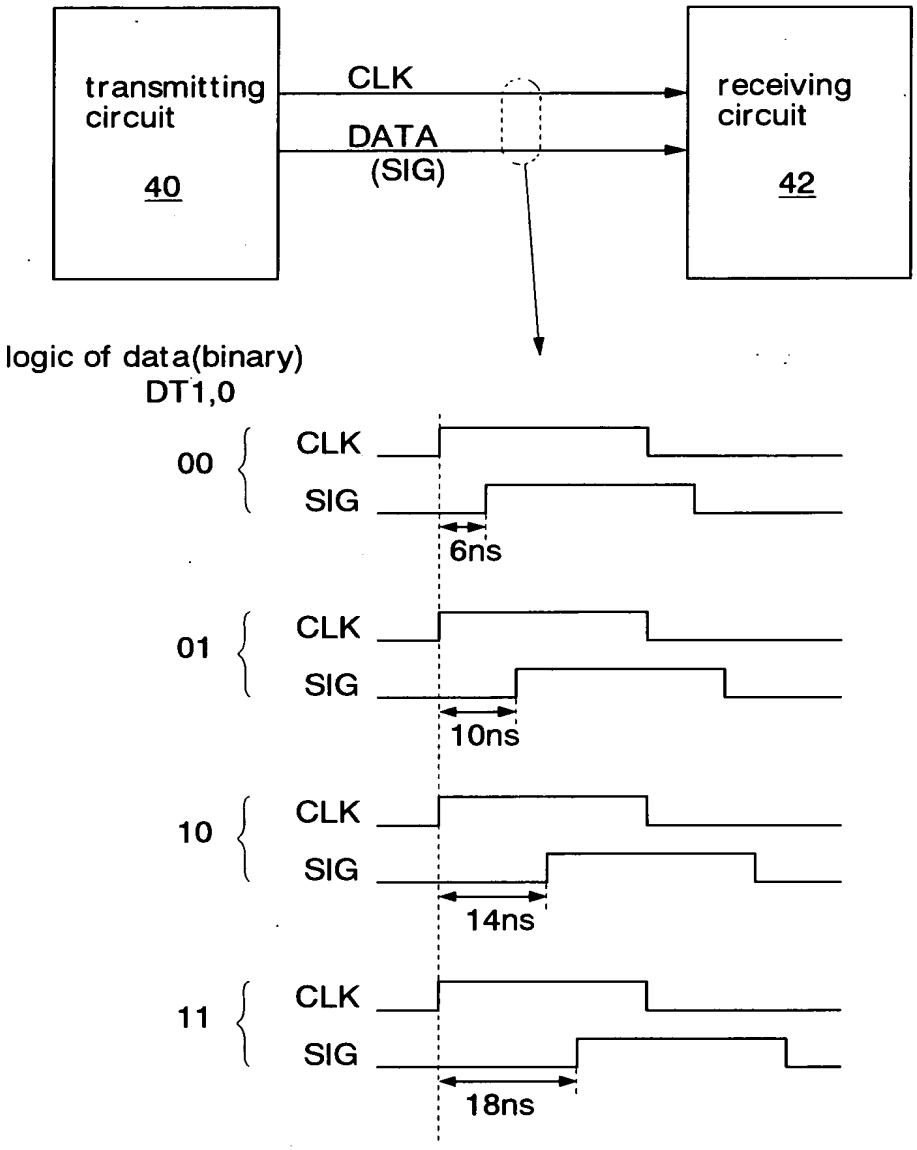

transmitting circuit
40
CLK
DATA
(SIG)
receiving circuit
42
logic of data(binary)
DT1,0
00
CLK
SIG
6ns
01
CLK
SIG
10ns
10
CLK
SIG
14ns
11
CLK
SIG
18ns

Fig. 13

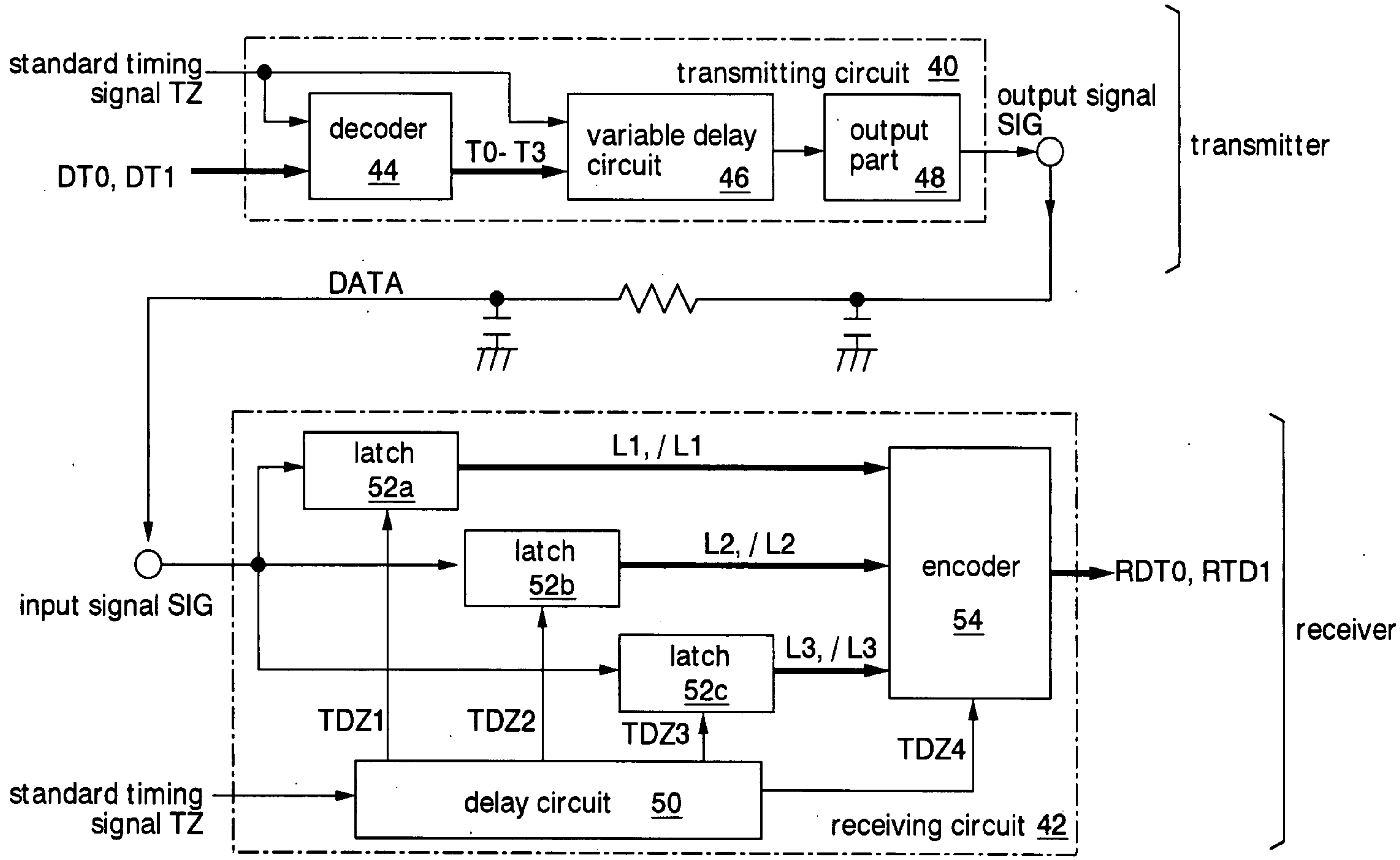

standard timing signal TZ
DT0, DT1
transmitting circuit 40
decoder 44
T0- T3
variable delay circuit 46
output part 48
output signal SIG
transmitter
DATA
latch 52a
latch 52b
latch 52c
L1, / L1
L2, / L2
L3, / L3
encoder 54
RDT0, RTD1
input signal SIG
receiver
TDZ1
TDZ2
TDZ3
TDZ4
standard timing signal TZ
delay circuit 50
receiving circuit 42

Fig. 14

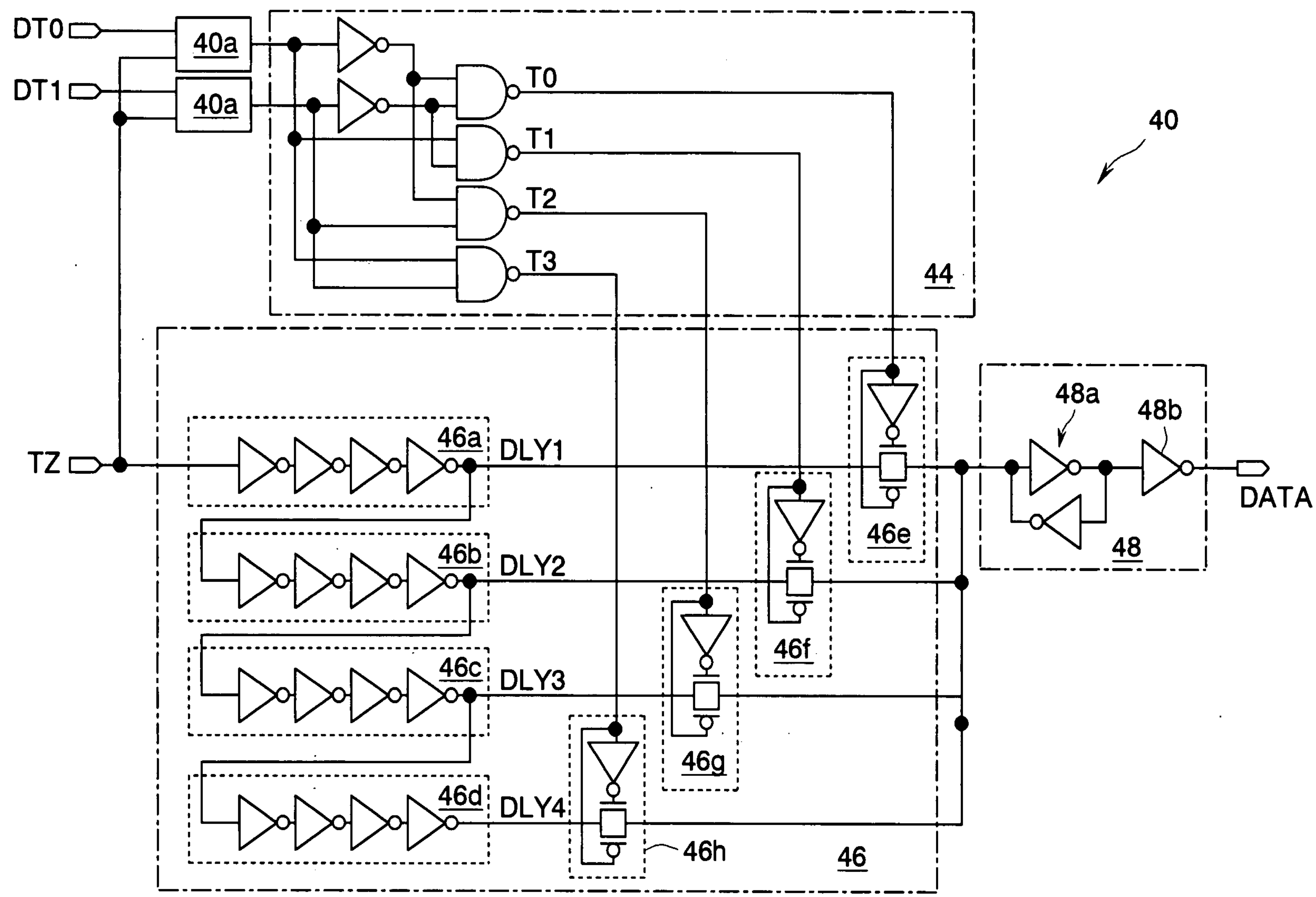

DT0
DT1
40a
40a
T0
T1
T2
T3
44
40
TZ
46a
DLY1
46b
DLY2
46c
DLY3
46d
DLY4
46e
46f
46g
46h
46
48a
48b
48
DATA

Fig. 15

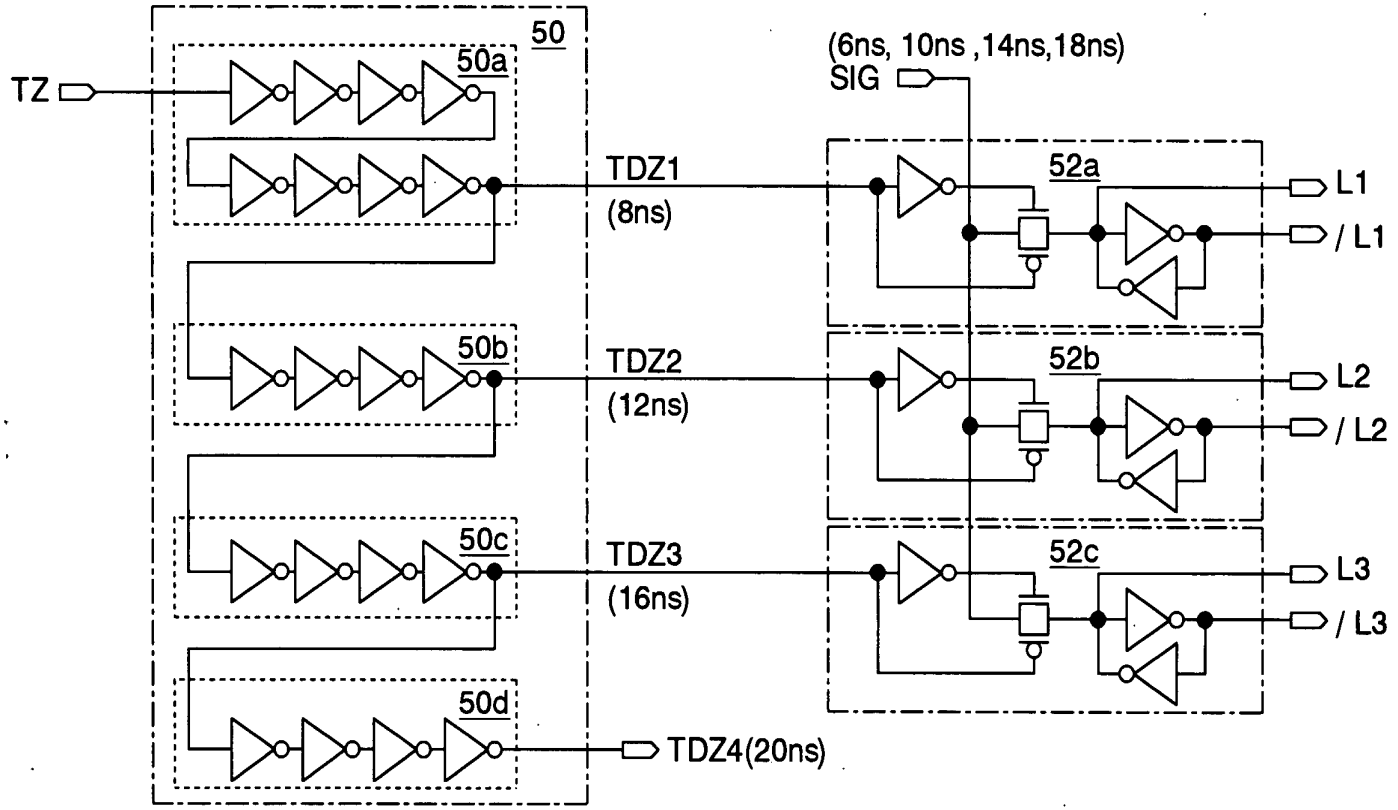


Fig. 16

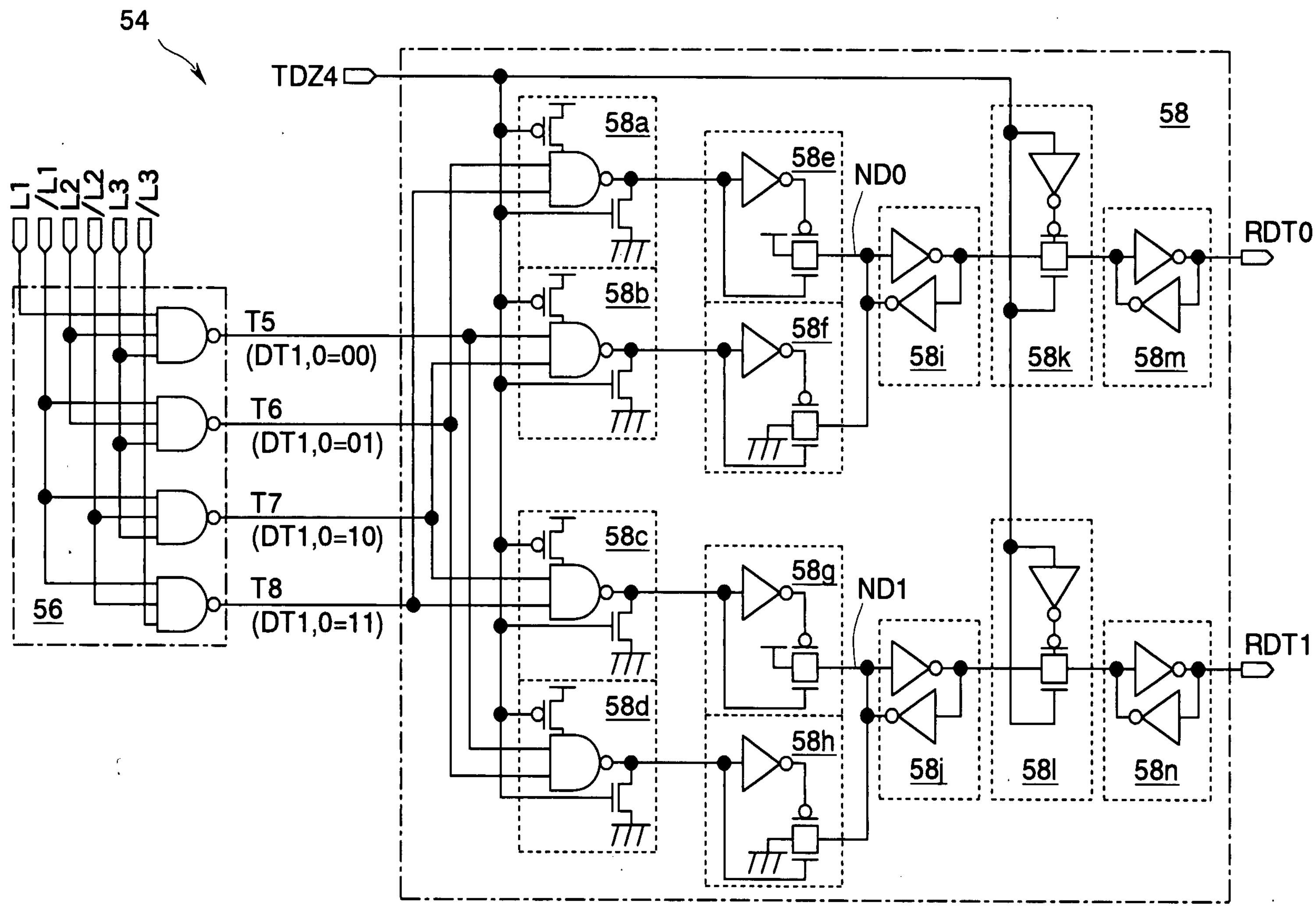

54
TDZ4
58
58a
58b
58c
58d
58e
58f
58g
58h
58i
58j
58k
58l
58m
58n
ND0
ND1
RDT0
RDT1
L1
/L1
L2
/L2
L3
/L3
T5
(DT1,0=00)
T6
(DT1,0=01)
T7
(DT1,0=10)
T8
(DT1,0=11)
56

Fig. 17

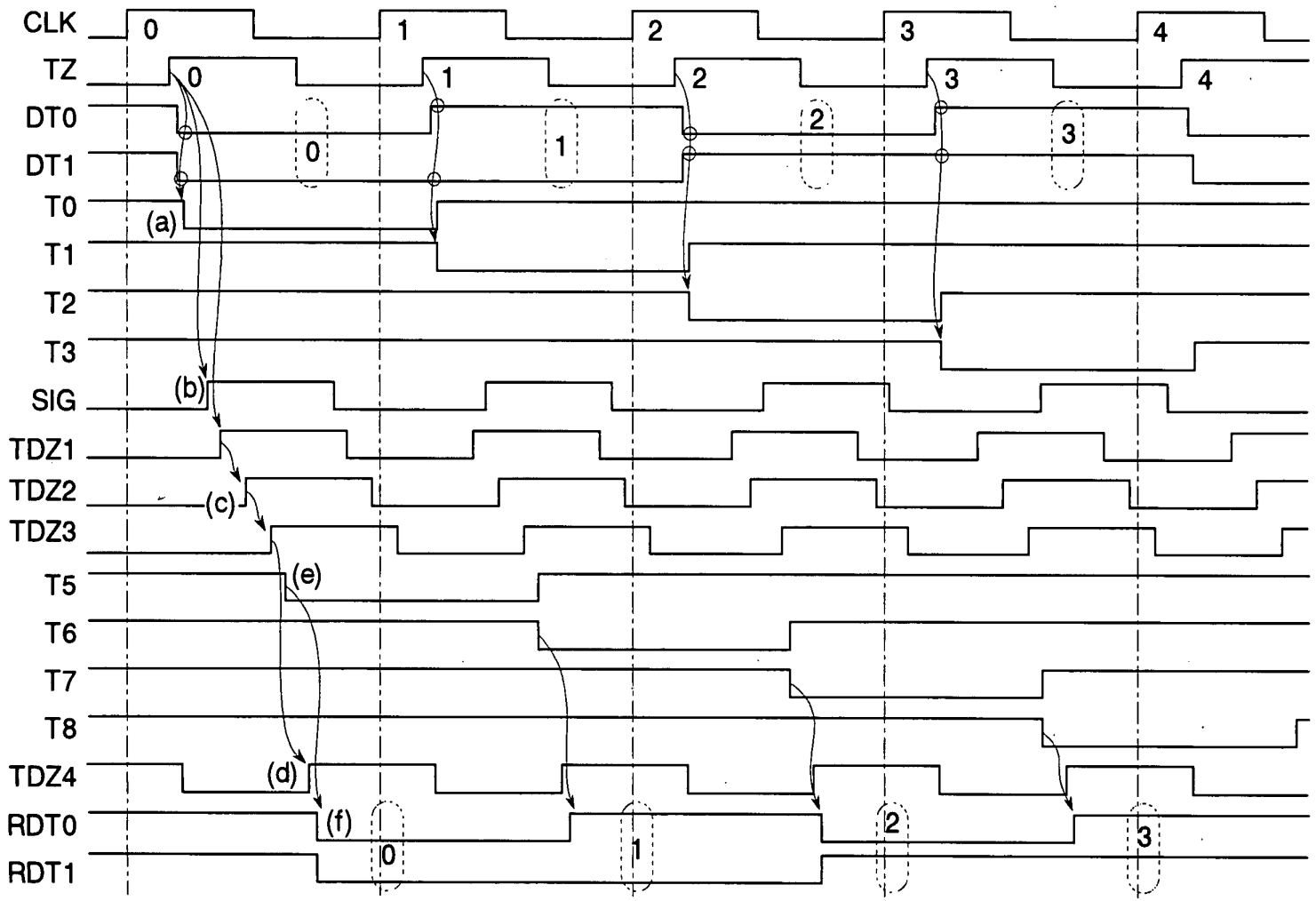


Fig. 18

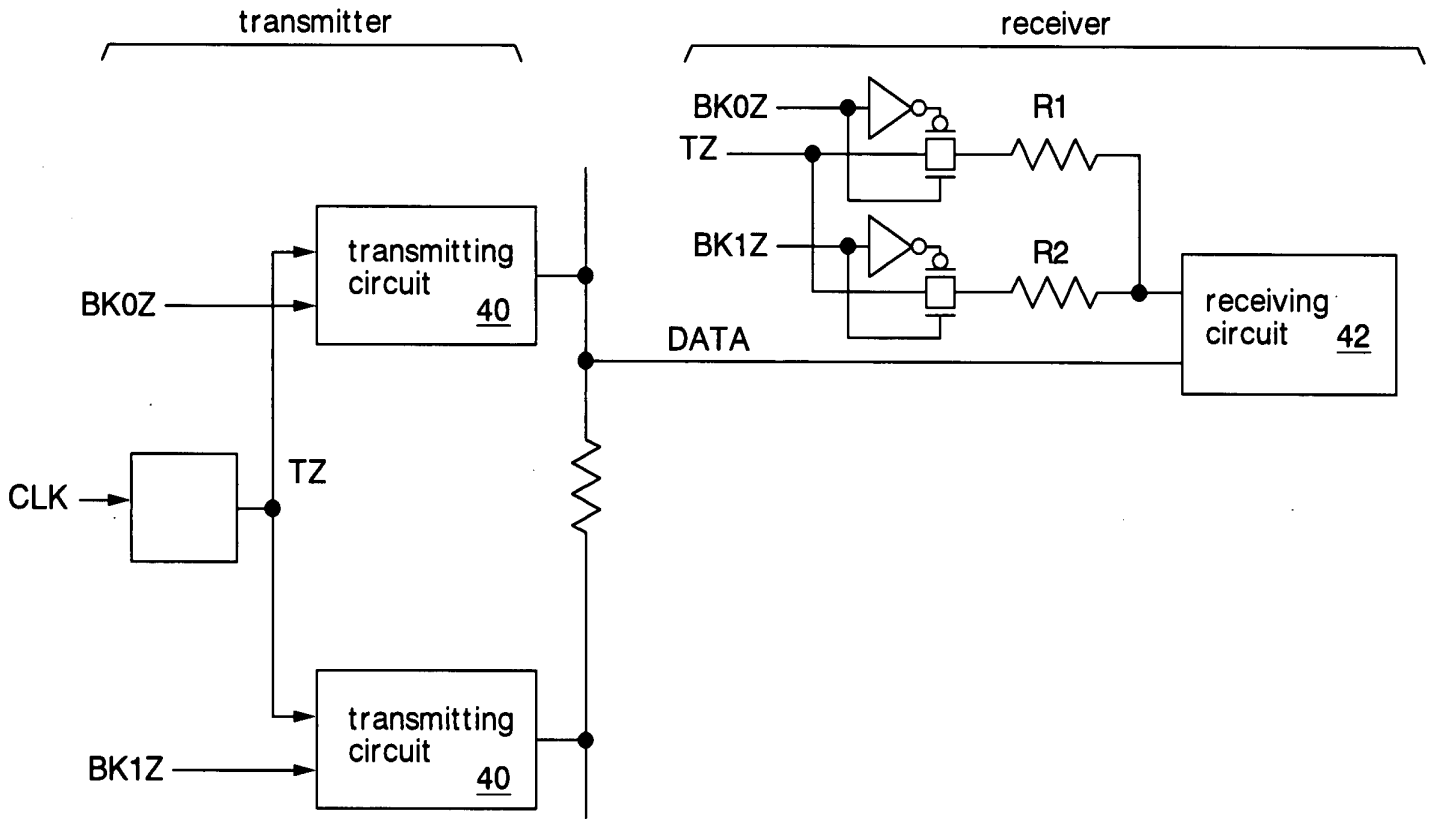

transmitter
receiver
BK0Z
TZ
BK1Z
R1
R2
transmitting circuit 40
BK0Z
DATA
receiving circuit 42
CLK
TZ
transmitting circuit 40
BK1Z

Fig. 19

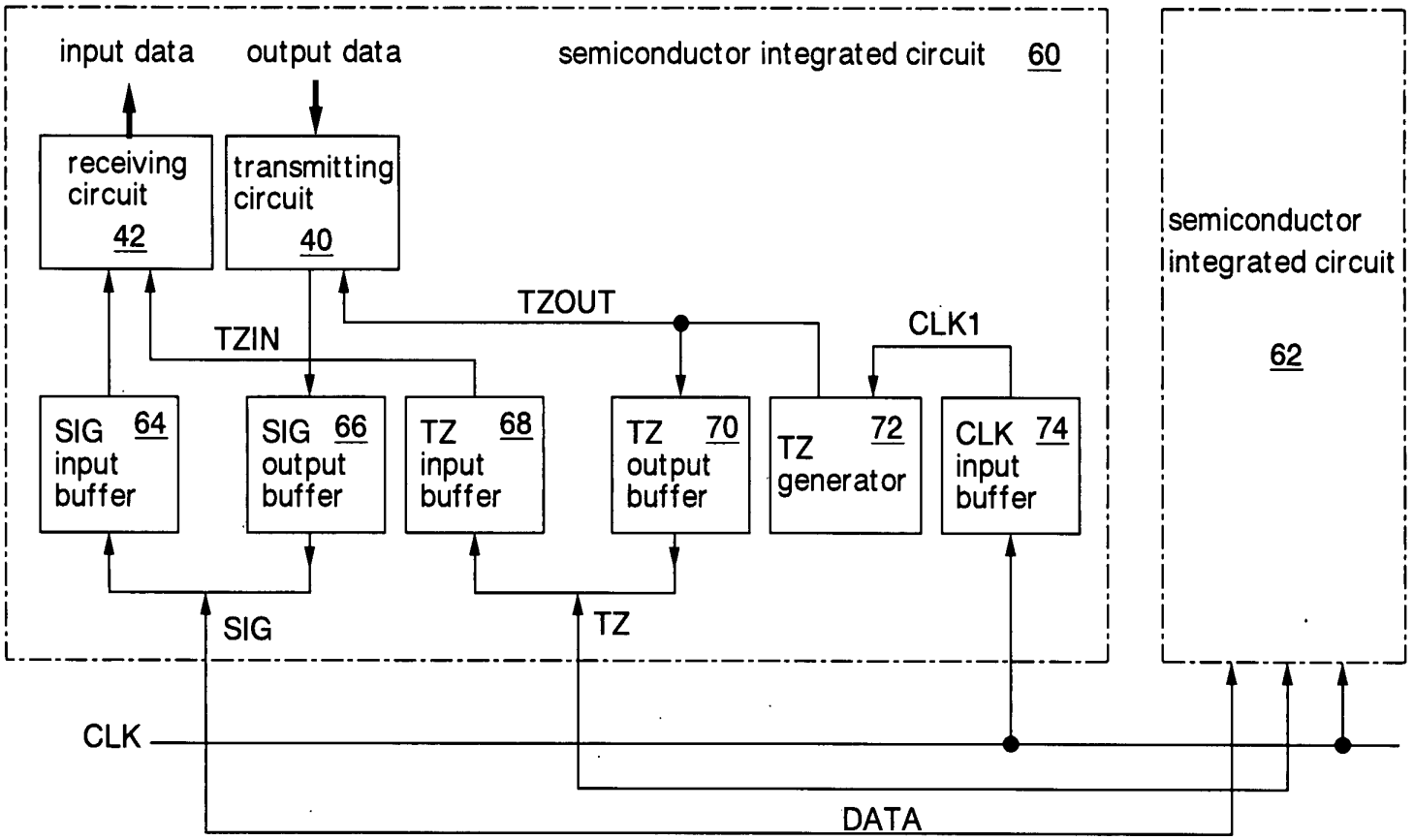

input data
output data
semiconductor integrated circuit 60
receiving circuit 42
transmitting circuit 40
semiconductor integrated circuit 62
TZOUT
CLK1
TZIN
SIG 64 input buffer
SIG 66 output buffer
TZ 68 input buffer
TZ 70 output buffer
TZ 72 generator
CLK 74 input buffer
SIG
TZ
CLK
DATA

Fig. 20

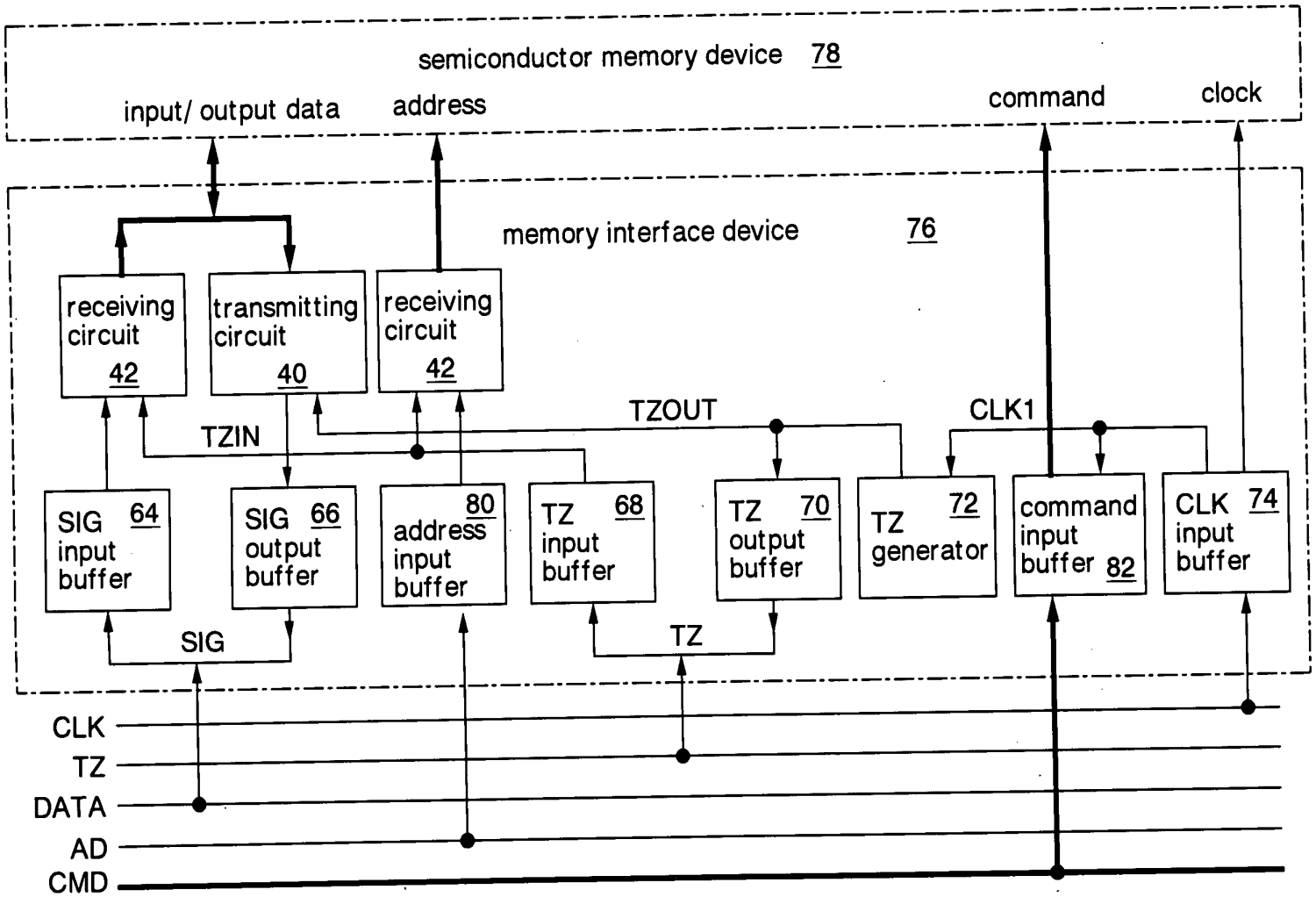


Fig. 21